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10/798,389	03/12/2004	Amid Hashim	4799/0112PUS1	6042

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EXAMINER	
NGUYEN, HOA CAO	
ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 10/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,389	HASHIM ET AL.	
	Examiner	Art Unit	
	Hoa C. Nguyen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 30-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 30-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2 pgs*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 8/18/06 has been entered. Applicants have amended claims 1, 2, 7, 10-11, and 15-17. Claims 18-29 are cancelled. Claims 30-33 are newly added.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the plurality of contacts, mating connector, and conductors of the mating connector must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-15 and 30-33 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. At least in claim 1, the claimed structure contains a plurality of contacts mounted on the PCB for contacting conductors of a mating connector, wherein at least some of the contacts are electrically connected to circuit elements formed on the PCB that were not described in the specification and also not described in the drawings. Claims 2-15 and 30-33 are dependent claims of claim 1.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1-17 and 30-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClanahan et al. (US 5396397) in view of Celella et al. (US 20040147165).

Regarding claim 1, as shown in figures 1-5, McClanahan discloses a multilayer printed circuit board (PCB) comprising:

(a) Circuit elements (any circuit traces/vias/pads shown in the figures; for example, conductive traces; see column 2, line 65);

(b) a plurality of contacts (at least, clearly shown on the outer layers of the PCB) mounted on the PCB for contacting conductors of a mating external discrete components (for example: discrete circuit devices, column 2, lines 61-62) mounted on the outside of the PCB, wherein at least some of the contacts are electrically connected to the external discrete elements, and wherein original crosstalk (unwanted noise - EMI interference) inherently occurs between at least some conductors of the mating external discrete components;

(c) a first section of the PCB (shaded layers, high dielectric field layers, col.4: 39-41) having a first dielectric constant (high DK, all shaded layers are high DK, col.3: 20-42);

(d) a second section of the PCB (unshaded layers – basic substrate insulating layers, col.4: 39-41) having a second DK lower than the first DK (col.4: 13-19), and provided above or below the first section (at least figures 3 and 5 show the high dielectric field layers are either sandwiched between the basic substrate insulating layers or in reversed order); and

(e) at least one crosstalk compensation element (capacitors, col.5: 17-58; col.4: 44-53;) utilizing the first section to provide compensating crosstalk to offset the original crosstalk (EMI interference, col.1:7-col.2:2), wherein the circuit elements are provided in the second section (all layers have circuit patterns; as shown in the figures and col.4: 44-53, including in the second section).

But, McClanahan fails to disclose a mating connector connecting to the PCB. Instead, McClanahan only discloses the plurality of contacts for discrete circuit devices mounted on the PCB (see figures 4-5).

However, a surface mounting connector formed on a surface of a PCB is old and well known in the art for connecting to external devices. Therefore, the surface mounting pads and vias shown in the figures can be used for connecting to a connector instead of only external discrete components.

Celella, as shown in figure 3 and paragraphs 20-21, discloses a printed circuit board 16 for providing crosstalk compensation comprising circuit traces formed therein

and at least a connector 14 (jack 14 - a modular jack) formed on the surface of the PCB 16 for connecting to an external communication device/system through a plug 12.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the teachings from Celcella to add a connector, such as connector 14 (a modular jack), on the surface of the PCB of McClanahan in order to connect to an external communication device, and thus extending operating applications of McClanahan's printed circuit board.

Examiner remarks:

It is noted that all printed circuit boards can be formed for modular connector. It is only a matter of choices depending upon particular applications. Furthermore, the recitation that a printed circuit board for a modular connector has not given patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. Kropa v. Robie, 88 USPQ 478 (CCPA 1951).

Moreover, the limitation that original cross talk occurs between at least some conductors of the mating connector and that the crosstalk compensation element utilizes the first section to provide compensating crosstalk to offset the original crosstalk is interpreted to only require the ability to so perform. In the case of product claim, only the structure of the claim distinguishes over the prior art.

Regarding claims 2-3, as shown in figure 5, McClanahan discloses every limitation as shown in claim 1 above including the first section, which comprises a first laminate including a substrate L6 having the first DK (high DK dielectric layer) and at least a metal sheet 67 attached to at least one surface of the substrate L6, and a first prepreg L5 above the first laminate.

But, McClanahan fails to disclose a second prepreg below the first laminate.

In a multilayer circuit board, it is well known in the art that the number of layers having the same dielectric constant is not limited to only one or two layers. It is totally depending upon particular applications. For example, as shown in figure 7, McClanahan discloses layers L3-L12 that are stacked on each other and each layer has the same dielectric constant (low DK); and, layers L4-L11 can be arbitrarily selected as a laminate layer, and layers L3 and L12 are arbitrary selected as a first prepreg and a second prepreg formed above and below the laminate layer respectively.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add more layers to the first section of McClanahan's circuit board such that a second prepreg having the same DK as the first laminate formed below the first laminate in order to add more components to the first section.

Regarding claim 4, McClanahan discloses the high dielectric constant field control layers in accordance with the invention that can also be printed with passive components, conductive traces, and conductive shields in the same manner as the basic insulating layers included in the multilayer circuit structure (col.5: 17-22). Therefore, McClanahan anticipates every limitation of the claim including the at least

one crosstalk compensation element (capacitors, see col3:23-58) is provided at a metal sheet (a circuit layer or ground or power layer) of the first laminate.

Regarding claim 5, at least as shown in figure 5, McClanahan discloses the second section (the unshaded layers, the basic substrate insulating layers), which includes:

(a) A third prepreg (namely L4) above the first prepreg (considering the top most layer L5 of the high DK layers as the first prepreg);

(b) a first metal layer (the conductive layer above L4 and below L3) above the third prepreg L4;

(c) a fourth prepreg (namely L7).below the second prepreg (considering the bottom layer L6 of the high DK as the second prepreg); and

(d) a second metal layer (the conductive layer below L7 and above L8) below the fourth prepreg.

Regarding claim 6, at least as shown in figure 5, McClanahan et al. disclose the third and fourth prepregs having the second DK (unshaded layers - the basic substrate insulating layers).

Regarding claim 7, at least as shown in figure 5, McClanahan discloses:

(a) The at least one circuit element (circuit pattern - conductive traces, vias as shown in the figures) is provided at the first and/or second metal layer, and

(b) at least a portion of the at least one crosstalk compensation element (capacitor and its electrodes - passive components) is inherently provided at a metal sheet and/or the substrate of the first laminate (col.5: 17-22 and col.3: 53-62).

Regarding claim 8, at least as shown in figure 5, McClanahan discloses the second section (the unshaded layers) includes:

(a) A second laminate L1-L4 (a lamination of a plurality of sheets/layers) above the first prepreg (considering the top most layer L5 of the high DK layers as the first prepreg); and

(b) a third laminate L7-L10 (a lamination of a plurality of sheets/layers) below the second prepreg (considering the bottom layer L6 of the high DK as the second prepreg),

(c) the second and third laminates have the second DK (unshaded layers - the basic substrate insulating layers).

Regarding claim 9, at least as shown in figure 5, McClanahan discloses each of the second and third laminates includes a dielectric material substrate (unshaded layers - the basic substrate insulating layers) and a single metal sheet (circuit pattern/conductive traces/ground/power layers) on the substrate.

Regarding claim 10, at least as shown in figure 5, McClanahan discloses:

(a) The at least one circuit element (circuit traces/vias is provided at the single metal sheet of the second and/or third laminate, and

(b) at least a portion of the at least one crosstalk compensation element (capacitors - its electrodes, see claim 7 above) is provided at a metal sheet and/or the substrate of the first laminate.

Regarding claims 11-12, at least as shown in figures 1-3, McClanahan discloses the second section (the basic substrate insulating layers), which includes:

(a) A first laminate including a substrate L4 having the second DK (considering middle layer L4 as a laminated layer of the basic substrate insulating layers, see figures 1-2 and 7-8 for example), and a metal sheet (circuit traces) attached to one surface of the substrate (see figure 1);

(b) a first prepreg L3 above the first laminate;

(c) a second prepreg L5 below the first laminate; and

(d) all unshaded layers are the second section having a second DK (see claim 1 above).

Regarding claim 13, as clearly shown in figure 3, McClanahan discloses the first section, which includes:

(a) A third prepreg L2 above the first prepreg;

(b) a first metal layer 35 (a conductive layer) above the third prepreg;

(c) a fourth prepreg L6 below the second prepreg; and

(d) a second metal layer 37 (a conductive layer) below the fourth prepreg.

Regarding claim 14, as clearly shown in figure 3, McClanahan discloses the third and fourth prepregs having the first DK (shaded layers).

Regarding claim 15, at least as shown in figure 3, McClanahan discloses:

(a) The at least one crosstalk compensation element (capacitor for example) is provided at the first and/or second metal layer (col.5: 17-58), and

(b) the at least one circuit element (any circuit element, circuit traces/vias for example) is provided at a metal sheet (a conductive layer in the basic substrate insulating layers) of the first laminate.

Regarding claim 16, as shown in figure 5, McClanahan et al. disclose a printed circuit board comprising:

(a) A first section L5/L6 (shaded layers) having a first dielectric constant (high DK);

(b) a second section L1-L4 having a second DK (low DK) lower than the first DK, and provided above the first section;

(c) at least one cross talk compensation element (capacitor, see col.1:23-27); and

(d) at least one circuit element (vias/metal traces) provided in the second section.

But, McClanahan fails to disclose the first DK in the range of 4:00-5:00 and the second DK in the range of 2.5-3.5.

However, McClanahan discloses that the choice of location and **material** for dielectric field control layers (and the basic substrate insulating layers, col. 7: 34-50) is highly dependent on the characteristics of the particular application including, for example, circuit geometry, operating frequencies, power level, and so forth (col.3: 53-62; col.7: 33-50). Thus, it is only a matter of choice for a particular application.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the first DK in the range of 4.0-5.0 and the second DK in the range of 2.5-3.5 in order to provide a predetermined capacitance for a specific application. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 17, as shown in figure 5, McClanahan et al. disclose a printed circuit board comprising:

(a) A first section L5/L6 (shaded layers) having a first dielectric constant (high DK);

(b) a second section L1-L4 having a second DK (low DK) lower than the first DK, and provided above the first section;

(c) at least one cross talk compensation element (capacitors, see col.1:23-27); and

(d) at least one circuit element (vias/metal traces) provided in the second section.

But, McClanahan fails to disclose the at least one crosstalk compensation element inherently include a plurality of capacitors places at different compensation stages of the PCB.

Capacitors are old and well known for filtering unwanted noise and the filter can be designed to contain multiple stages of filtering. Thus, it is only a matter of design choice depending upon particular application.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include a plurality of filtering stages formed in the PCB in order to surely canceling any unwanted noise. Furthermore, it has been held that the provision of adjustability, where needed, involves only routine skill in the art. *In re Stevens*, 101 USPQ 284 (CCPA 1954).

Regarding claim 30, McClanahan discloses every limitation as shown in claim 1 above.

But, McClanahan fails to disclose the first DK in the range of 4.0-5.0 and the second DK in the range of 2.5-3.5.

However, McClanahan does disclose that the choice of location and **material** for dielectric field control layers (and also the basic substrate insulating layers, col.7: 34-50) is highly dependent on the characteristics of the particular application including; for example, circuit geometry, operating frequencies, power level, and so forth (col.3: 53-62; col.7: 33-50). Thus, it is only a matter of choice depending upon particular applications.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the first DK in the range of 4.0-5.0 and the second DK in the range of 2.5-3.5 in order to provide a predetermined capacitance for a specific application. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claims 31-32, McClanahan discloses every limitation as shown in claim 1 above.

But, McClanahan fails to disclose the at least one crosstalk compensation element, which includes a plurality of capacitors places at different compensation stages of the PCB.

Capacitors are old and well known for filtering unwanted noise and the filter can be designed/arranged to contain multiple stages of filtering, wherein each stage must

contain at least one capacitor (the key component for forming a filter). Thus, it is only a matter of design choice depending upon particular applications.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include a plurality of filtering stages, wherein each stage inherently contains at least one capacitor, formed in the PCB in order to surely canceling a predetermined range of unwanted noise. Furthermore, it has been held that the provision of adjustability (from one application to another), where needed, involves only routine skill in the art. *In re Stevens*, 101 USPQ 284 (CCPA 1954).

Regarding claim 33, McClanahan in view of Celella discloses every limitation as shown in claim 1 above.

Response to Arguments

8. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reichard Dean can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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